IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please CANCEL claims 1 and 6 and AMEND claims 2-3 in accordance with the following:

1. (CANCELLED)

2. (CURRENTLY AMENDED) The digital phase locked circuit as claimed in claim ~~1~~5, wherein said phase comparison result detecting part~~, comprising~~ comprises:

an up-down counter counting up/down when a phase comparison signal, comprising an exclusive OR signal of said input clock signal and said output clock signal from said phase comparing part, is HIGH/LOW, respectively; and

a detecting part outputting a decreasing (DEC) request signal when a minimum counter value of said up/down counter is detected and an increasing (INC) request signal when a maximum counter value of said up/down counter is detected.

3. (CURRENTLY AMENDED) The digital phase locked circuit as claimed in claim ~~1~~5, wherein said execution rate computing part has a phase difference computing counter counting up/down a phase difference counter value thereof based on said INC/DEC request signal, respectively from said phase comparison result detecting part and setting said phase difference counter value as a computed phase difference and a phase absorption execution rate determining part outputting an execution rate corresponding to said computed phase difference with reference to a correspondence table in which correspondence between phase differences and execution rates is stored.

4. (ORIGINAL) The digital phase locked circuit as claimed in claim 3, wherein said execution rate computing part sets said computed phase difference by summing up a plurality of counter values for each predetermined time interval, the counter values computed by sampling said phase difference counter in a shorter time interval.

5. (PREVIOUSLY PRESENTED) A digital phase locked circuit for synchronizing a phase of a divided clock signal with a phase of an input clock signal wherein said divided clock signal is generated by dividing a master clock signal, comprising:

a phase comparing part comparing the phase of said output clock signal with the phase of said input clock signal;

a phase comparison result detecting part referring to a comparison result from said phase comparing part and outputting a signal increasing/decreasing a division number for dividing said master clock signal when the phase of said output clock signal proceeds forward/behind the phase of said input clock signal;

a mask processing part identifying a single applied mask rate among a plurality of mask rates for masking a part of an increasing/decreasing (INC/DEC) request signal depending on a phase difference between the input clock signal and the master clock signal, wherein as the phase difference increases, the mask rate is made lower, and as the phase difference decreases, the mask rate is made higher, masking the output signal from the phase comparison result detecting part depending on the identified mask rate, and outputting the masked signal; and

a dividing part obtaining the divided clock signal by controlling increasing or decreasing operation on the division number based on the outputted masked signal.

6. (CANCELLED)